AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A phase error correction circuit for correcting a phase error in an input signal having a frame structure containing a preamble, a ~~specific pattern~~ unique word, and data, said phase error correction circuit comprising:

a correction value calculation section for calculating a phase correction value based on a predetermined number of symbols contained in the preamble of the input signal;

a correction value determination section for retaining, with a ~~predetermined~~ timing at which a specific pattern contained in the unique word is detected, a phase correction value calculated by the ~~phase~~ correction value calculation section ~~section, based on the predetermined number of symbols contained in the preamble~~;

a phase rotation section for subjecting the input signal to a phase rotation process using the phase correction value retained in the correction value determination section; and

a specific pattern detection section for detecting the specific pattern contained in an output signal from the phase rotation section ~~to output a specific pattern detection signal~~, and outputting a result of the detection to the correction value determination section

~~wherein the correction value determination section retains the phase correction value calculated by the correction value calculation section with a timing determined based on the specific pattern detection signal~~.

2. (Currently Amended) The phase error correction circuit according to claim 1, wherein,

the correction value determination section outputs the phase correction value calculated by the correction value calculation section to the phase rotation section without retaining the phase correction value until the specific pattern is detected ~~retaining the phase correction value calculated by the correction value calculation section with the predetermined timing~~, and

~~until the correction value determination section retains the phase correction value calculated by the correction value calculation section with the predetermined timing,~~ the phase rotation section subjects the input signal to a phase rotation process using the phase correction value which is output from the correction value determination section until the specific pattern is detected.

3. (Original) The phase error correction circuit according to claim 1, further comprising an alternation detection section for outputting an alternation detection signal indicating inversions of a sign of the input signal from symbol to symbol.

4. (Original) The phase error correction circuit according to claim 3, wherein the correction value calculation section calculates the phase correction value with respect to a portion of the input signal for which the alternation detection signal is output.

5. (Original) The phase error correction circuit according to claim 1, wherein the correction value calculation section includes:

a phase inversion section for inverting a phase of the input signal from symbol to symbol;

a mean value calculation section for calculating a mean value of the predetermined number of symbols in an output signal from the phase inversion section; and

a mean value inversion section for inverting, depending on a sign of an output signal from the mean value calculation section, the sign of the output signal.

6. (Original) The phase error correction circuit according to claim 5, wherein the mean value calculation section calculates the mean value by cumulatively adding the output signal from the phase inversion section by using one symbol adder, such that one mean value is calculated per plurality of symbol periods.

7. (Original) The phase error correction circuit according to claim 5, wherein the mean value calculation section calculates the mean value by cumulatively adding the output signal from the phase inversion section by using a plurality of symbol adders in parallel, such that one mean value is calculated per symbol period.

8. (Original) The phase error correction circuit according to claim 7, further comprising a delay section for delaying the input signal supplied to the correction value calculation section by a predetermined amount of time from the input signal supplied to the phase rotation section,

wherein the predetermined amount of time is determined so that the specific pattern is detected by the specific pattern detection section while the correction value calculation section is calculating the phase correction value with respect to the preamble contained in the input signal.

9. (Original) The phase error correction circuit according to claim 1, wherein the correction value determination section retains the phase correction value calculated by the correction value calculation section based on the predetermined number of symbols including the last symbol of the preamble.

10. (Currently Amended) The phase error correction circuit according to claim 1, wherein the correction value determination section includes:

a correction value storage section for storing a plurality of phase correction values calculated by the correction value calculation section in a chronological order;

a correction value selection section for selecting one of the phase correction values stored in the correction value storage section; and

a correction value retention section for~~, based on the specific pattern detection signal,~~ fetching and retaining the phase correction value selected by the correction value selection section with the timing at which the specific pattern is detected, and stopping fetching the phase correction value after ~~the specific pattern detection signal is output~~ the timing at which the specific pattern is detected.

11. (Original) The phase error correction circuit according to claim 10, wherein the correction value selection section receives an indication of a number of correction values to go back, and from among the phase correction values stored in the correction value storage section, selects and outputs a phase correction value as designated by the number of correction values to

go back.

12. (Original) The phase error correction circuit according to claim 10, further comprising an end detection section for detecting an end portion of the data contained in the input signal to output an end detection signal,

wherein the correction value retention section starts fetching the phase correction value after a predetermined amount of time since the end detection signal is output.

13. (Currently Amended) The phase error correction circuit according to claim 1, wherein the correction value determination section stops fetching the phase correction value after ~~the specific pattern detection signal is output~~ the timing at which the specific pattern is detected.

14. (Original) The phase error correction circuit according to claim 13, further comprising an end detection section for detecting an end portion of the data contained in the input signal to output an end detection signal,

wherein the correction value determination section starts fetching the phase correction value after a predetermined amount of time since the end detection signal is output.

15. (Original) The phase error correction circuit according to claim 1, further comprising a 45° rotation section for rotating a phase of the input signal supplied to the correction value calculation section by 45°.

16. (Canceled)

17. (Currently Amended) A receiver for receiving a digitally-modulated signal, the receiver comprising:

a detector section for detecting a received signal having a frame structure containing a preamble, a unique word, and data;

a clock recovery section for recovering a clock signal from an output signal from the detector section while switching zero cross reference axes based on a given control signal; and

a phase error correction circuit for correcting a phase error in an output signal from the detector section for which judging points have been determined based on the clock signal recovered by the clock recovery section, and supplying phase error information indicating a magnitude of the phase error as the control signal to the clock recovery section,

~~The receiver according to claim 16, wherein,~~

~~the received signal is a signal having a frame structure containing a preamble, a specific pattern, and data, and~~

wherein the phase error correction circuit comprises:

a correction value calculation section for calculating a phase correction value based on a predetermined number of symbols contained in the preamble of the output signal from the detector section;

a correction value determination section for retaining, with a ~~predetermined~~ timing at which a specific pattern contained in the unique word is detected, a phase correction value

calculated by the ~~phase~~ correction value calculation section~~, based on the predetermined number of symbols contained in the preamble~~;

a phase rotation section for subjecting the output signal from the detector section to a phase rotation process using the phase correction value retained in the correction value determination section; and

a specific pattern detection section for detecting the specific pattern contained in an output signal from the phase rotation section ~~to output a specific pattern detection signal~~, and outputting a result of the detection to the correction value determination section

~~wherein the correction value determination section retains the phase correction value calculated by the correction value calculation section with a timing determined based on the specific pattern detection signal~~.

18. (Canceled)

19. (Currently Amended) A receiver for receiving a digitally-modulated signal, the receiver comprising:

a detector section for detecting a received signal having a frame structure containing a preamble, a unique word, and data;

a phase error correction circuit for correcting a phase error in an output signal from the detector section using a given clock signal; and

a clock recovery section for, based on a signal which has been corrected by the phase

error correction circuit, recovering a clock signal to be used for demodulating the signal, and supplying the recovered clock signal to the phase error correction circuit,

~~The receiver according to claim 18, wherein,~~

~~the received signal is a signal having a frame structure containing a preamble, a specific pattern, and data, and~~

wherein the phase error correction circuit comprises:

a correction value calculation section for calculating a phase correction value based on a predetermined number of symbols contained in the preamble of the output signal from the detector section;

a correction value determination section for retaining, with a ~~predetermined~~ timing at which a specific pattern contained in the unique word is detected, a phase correction value calculated by the ~~phase~~ correction value calculation section~~, based on the predetermined number of symbols contained in the preamble~~;

a phase rotation section for subjecting the output signal from the detector section to a phase rotation process using the phase correction value retained in the correction value determination section; and

a specific pattern detection section for detecting the specific pattern contained in an output signal from the phase rotation section ~~to output a specific pattern detection signal~~, and outputting a result of the detection to the correction value determination section

~~wherein the correction value determination section retains the phase correction value calculated by the correction value calculation section with a timing determined based on the~~

~~specific pattern detection signal~~.

20. (Currently Amended) A signal transmission method for transmitting data in frames, the method comprising ~~the steps of~~:

~~splitting data to be transmitted into units of a predetermined length;~~

generating a frame-structured data by adding, in front of ~~each unit of split~~ data to be transmitted which is split into units of a predetermined length, a preamble which alternates from symbol to symbol, and a specific pattern selected so as not to allow a predetermined length of symbol-to-symbol alternations to occur even in the presence of a symbol error; and

subjecting the frame-structured data to digital modulation and transmitting the modulated frame-structured data.